Arda Caliskan

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EDUCATION

University of Southern California, Viterbi School of Engineering August 2024–May 2030
PhD in Computer Engineering
University of Southern California, Viterbi School of Engineering August 2023–May 2024
Master of Science in Electrical and Computer Engineering GPA – 3.80
University of Southern California, Viterbi School of Engineering August 2020–May 2024
Bachelor of Science in Electrical and Computer Engineering GPA – 3.93

Honors: Dean's List
Activities and Societies: USC Formula Electric, IEEE
Relevant Coursework: Complex Digital ASIC System Design, Advanced Topics in Microarchitecture, MOS VLSI Circuit Design, Computer Systems Architecture, Systems for Machine Learning, Computer Systems Organization

SKILLS & INTERESTS

Software: C++, C, Verilog, Linux, Python, Pytorch, Cadence Virtuoso, gem5, MATLAB
Hardware: ASIC Design, Computer Architecture, VLSI Design GPU/CPU architecture, Embedded Systems, PCB design

EXPERIENCE

SPORT Lab – Research Assistant September 2023–Present

- Designing and optimizing digital superconducting circuits for use in an energy efficient superconducting CPU design.
- Simulating superconducting logic cells containing Josephson Junctions and inductors using JoSIM.
- Drawing and extracting superconducting layouts using Cadence Virtuoso and InductEx.

USC Formula Electric - Systems Electrical Lead August 2022–Present

- Taking a leading role in creating SC Formula Electric's first-ever fully operational electric competition race car.
- Actively participating in the recruitment and successful integration of new team members.
- Facilitating seamless collaboration with other subteams to ensure the harmonious functioning of all electrical systems, compliance with regulations, and physical integration with the vehicle's overall structure.
- Managing and supervising the testing and wiring of critical high and low voltage systems and spearheading schematic design and fabrication using **KiCad**.

USC – Teaching Assistant, Introduction to Digital Circuits August 2024–Present

- Working as a Teaching Assistant for an introductory digital circuits lab section involving **Verilog** coding for **FPGAs.**
- Holding lab sections with 20+ students to assist in designing and debugging various digital state machines and in-order CPU designs.

RECENT PROJECTS

A 16nm XGCD Accelerator ASIC (Intel University Shuttle Program) August 2024

- Designing and building an extended greatest common divisor (XGCD) **ASIC** optimized for area and energy efficiency for applications in resource efficient blockchains and DDoS secure networks.
- Learning Cadence & Synopsys EDA tools for synthesis, P&R, DRC, LVS, STA, and multi-corner timing checks.

LLM Training Project November 2023

- Implemented and trained a large language model using the **LLaMA** architecture.
- Optimized memory usage using automatic mixed-precision, low-rank adaptation, and gradient checkpointing to enable the model to fit inside a single GPU.
- Fine-tuned the model using the Alpaca dataset.

Cadence VLSI Project May 2023

- Designed a 20-bit adder-accumulator in **Cadence Virtuoso**, producing the best design in the class.
- Strategically tweaked the design to achieve the optimal balance between area and delay.
- Thoroughly assessed various logic families to maximize the chosen metric, and meticulously optimized the layout to minimize overall area utilization.

Pacman FPGA Project November 2022

- Wrote Verilog code for an FPGA-based Pacman game, seamlessly integrating it with a VGA interface.
- Incorporated a pseudo-random algorithm to infuse variability into the gameplay experience.